48 EASY STEPS TO THE JEM-X ON-BOARD EVENT PROCESSING

	PROCESSING STEP	PARAMETERS REQUIRED	#parm	HK-pos	COMMENTS	#instr.
	DATA INPUT AND INITIAL SELECTION STEPS					
1	Datainput: slow, fast, veto, time + some more					100
2	if (slow > slowmax) reject1	slowmax	1	104	Amplitude check - rejects particles	2
3	if (slow < slowmin) reject2	slowmin	1	104	Rejects out-of limits events	2
4	if (slow > 2 * fast) reject3			108	Risetime check - rejects particles	5
5	Datainput: complete c[0:10] and b[0:19]					150
6	Apply offset and gain corrections to slow, fast and veto	k_off[0:2], k_gain[0:2]	6			12
7	if (slow < k_vt * veto) reject4	k_vt	1	106	Crude veto-reject	5
8	Set isl = int(slow/k_fs); fsl = frac(slow/k_fs);	k_fs	1		Prepare for interpolation step*	10
9	if (slow > k_sl and fast < k_sp1[isl] + fsl * m_sl1[isl]) reject5	k_sp1[0:11], m_sl1[0:10], k_sl	13	112	Fine risetime-reject**	12
10	Set jsl = int(slow/k_kink); gsl = frac(slow/k_kink);	k_kink	1			10
11	if (slow < k_sl and fast < k_sp2[jsl] + gsl * m_sl2[jsl]) reject5	k_sp2[0:14], m_sl2[0:13]	15	112	Fine risetime-reject**.	12
12	if (slow > k_su and fast > k_sp3[isl] + fsl * m_sl3[isl]) reject5	k_sp3[0:11], m_sl3[0:10], k_su	13	110	Fine risetime-reject**	12
13	if (slow < k_su and fast > k_sp4[jsl] + gsl * m_sl4[jsl]) reject5	k_sp4[0:14], m_sl4[0:13]	15	110	Fine risetime-reject**.	12
	CATHODE POSITION					
14	Apply gain/offset to cathode signals and find max. signal	k_off[3:13], k_gain[3:13]	22		max signal: cmax, max position: ic	84
15	Define right & left positions modulo 11. [Ic2r, icr, ic, Icl, ic2l]					16
16	Set left/right_weight to: wlr = (c[ic2l] - c[ic2r]) * k_w / slow	k_w	1			9
17	Truncate wlr to interval: 0.0 < wlr < 1.0					6
18	Set: slow_r = slow * (1 - wlr); slow_l = slow * wlr;					8
19	Correct for anode-cathode coupling on 3 central positions: ….					
20	….. ccor[j] = c[j] + k_l[j,ic]*slow_l + k_r[j,ic]*slow_r; j=0,1,2	k_l[0:2][0:10], k_r[0:2][0:10]	66		this step repeated for j=0, 1 and 2	36
21	Verify local max. position, if new: repeat steps 15-20 (once!)				watch out for an endless loop here!	10
22	Set: ctot = ccor[0] + ccor[1] + ccor[2];					8
23	Set: dcpos = k_cimp * (ccor[2] - ccor[0]) / ctot;	k_cimp	1			7
24	If (dcpos < -k_w) dcrpos = k_sl1 * dcpos - m_step; skip to 27;	k_w, k_sl1, m_step***	2			4
25	If (dcpos > k_w) dcrpos = k_sl1* dcpos + m_step; skip to 27;					4
26	Set: dcrpos = k_sl2 * dcpos;	k_sl2	1			5
27	Set: cpos = (ic + dcpcr + 1) modulo 11					8
	REFINED SELECTION STEPS					
28	Set: dcrp1 = frac(cpos) - 0.5; dcrp2 = dcrp1 * dcrp1;					10
29	Set: ctsrat = ctot / slow;					4
30	Set jsl = int(cpos/k_cpint); gsl = frac(cpos/k_cpint);	k_cpint	1			10
31	if (ctsrat < k_cp1[jsl] + gsl * m_cp1[jsl]) reject6	k_cp1[0:54], m_cp1[0:53]	55	122	cathode "footprint" rejection	12
32	if (ctsrat > k_cp2[jsl] + gsl * m_cp2[jsl]) reject7	k_cp2[0:54], m_cp2[0:53]	55	120	cathode "footprint" rejection	12

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	PROCESSING STEP	PARAMETERS REQUIRED	#parm	HK-pos	COMMENTS	#instr.
33	Set: vetorat = veto / slow;					4
34	if (vetorat > k_vt1[jsl] + gsl * m_vt1[jsl]) reject8	k_vt1[0:54], m_vt1[0:53]	55	112	veto signal fine rejection	12
	BACKSIDE POSITION DETERMINATION					
35	Set: boff3 = k_boff0 + k_boff1 * dcrp1 + k_boff2 * dcrp2;	k_boff0, k_boff1, k_boff2	3		backside induced effects	9
36	Apply gain/offset to backside signals and find max. signal	k_off[14:33], k_gain[14:33]	40		max signal: bmax, max position: ib	160
37	Define right & left positions modulo 20. [ibr, ib, Icl]					8
38	Set: btot = b[ibl] + b[ib] + b[ibr] - boff3					11
39	Set: dbpos = k_bimp * (b[ibr] - b[ibl]) / btot	k_bimp	1			8
40	Set: bpos = (ib + dbpos + 1) modulo 20;					9
	BACKSIDE SELECTION					
41	Set dbrp1 = frac(bpos*2) - 0.5; ib2 = bpos * 2 - dbrp1;					14
42	Set btrat = btot / slow;					4
43	Set jsl = int(bpos/k_bpint); gsl = frac(bpos/k_bpint);	k_bpint	1			10
44	if (btrat < k_bp1[jsl] + gsl * m_bp1[jsl]) reject9	k_bp1[0:39], m_bp1[0:38]	40	118	backside "footprint" selection	12
45	if (btrat > k_bp2[jsl] + gsl * m_bp2[jsl]) reject10	k_bp2[0:39], m_bp2[0:38]	40	116	backside "footprint" selection	12
	OUTPUT PREPARATION					
46	Set: ecor = k_ecor0 + k_ecor1 * dcrp1 + k_ecor2 * dcrp2;	k_ecor0, k_ecor1, k_ecor2	3		induced effects in the energy signal	10
47	Set: slowout = slow / ecor;				0 < slowout < 4095	4
48	Set: xout = cpos * k_x; yout = cpos * k_y;	k_x, k_y	2		0 < xout < 1023, 0 < yout < 1023	4
	PARAMETER & INSTRUCTION COUNT TOTALS		456			888

Notes:
*) All detailed selection steps uses limits derived through linear interpolation from parameter tables
**) the m_xxx arrays and variables are not counted in the parameter count as they are derived on-board from the k_arrays and variables.
m_xxx[i] = k_xxx[i+1] - k_xxx[i]; 0 <= i <= N-1, where N is the dimension of the k_xxx array.
'***) m_step = k_sl2 * k_w;

Updated DFEE housekeeping usage reflecting the new event selection strategy and including a channel reporting the active CPU configuration.

DFEE Housekeeping Note: The following is an exact copy of the HK block received from DFEE.

Start (byte.bit#)	Size (bits)		Up-dated
82	16	HK Cycle Counter	
84	16	DFEE State	
86	8	Low Level Discriminator	
87	8	Anode configuration	
88	16	Delta HV monitoring, (dV)	
90	16	Cathode HV monitoring, (V_C)	
92	4	Cathode HV setting, (V_C), high order 4 bits	
92,4	4	delta HV setting, (dV), high order 4 bits	
93	4	delta HV setting, (dV), low order 4 bits	
93,4	4	Cathode HV setting, (V_C), low order 4 bits	
94	16	Number of software processed event triggers	
96	16	Number of accepted events	
98	16	Number of events rejected by grey filter	
100	16	Number of events rejected due to lack of buffer space	
102	16	Number of events rejected due to FIFO full	
104	16	Number of events rejected by upper threshold	
106	16	Number of events rejected by Veto Signal (crude)	x
108	16	Number of events rejected by Low Risetime (crude)	x
110	16	Number of events rejected by Risetime (fine)	x
112	16	Number of events rejected by Veto signal (fine)	x
114	16	Not used	x
116	16	# of events rejected by too high signal in Back Plane peak	x
118	16	# of events rejected by too low signal in Back Plane peak	x
120	16	# of events rejected by too high signal in Cathode Plane peak	x
122	16	# of events rejected by too low signal in Cathode Plane peak	x
124	16	Calibration spectrum partition number	
126	32x16	32 words of calibration spectrum	
190	16	CPU Mhz/waitstates: 0: 8/1; 1: 8/0; 2: 16/1; 3: 16/0	x
192	16	Hardware event trigger counter (wrap around counter, never reset) (Also enabled when DFEE is in SETUP state)	
194	16	Spare#3 = 16#AAAA#	